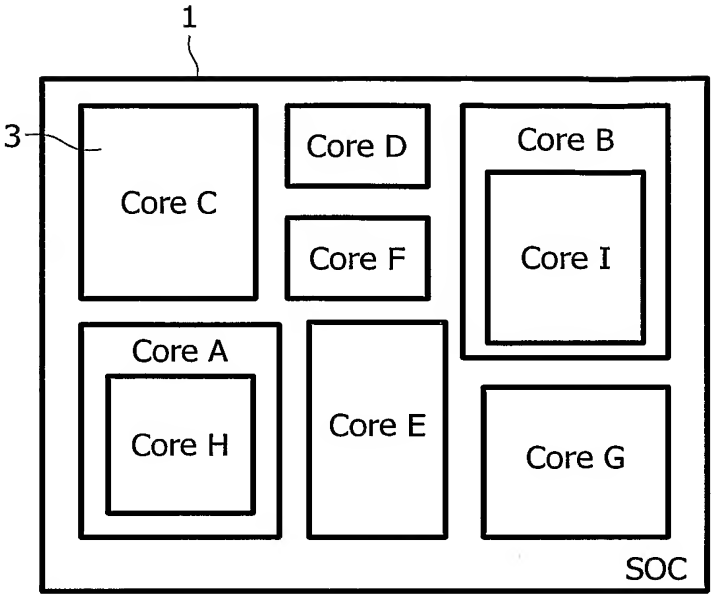

1
3
Core C
Core D
Core F
Core B
Core I
Core A
Core H
Core E
Core G
SOC

FIG. 1

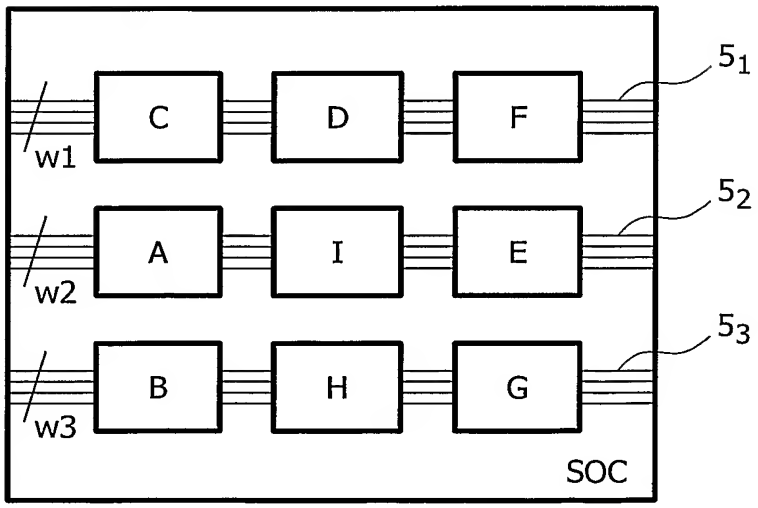

C
D
F
w1
A
I
E
w2
B
H
G
w3
SOC
5_1
5_2
5_3

FIG. 2

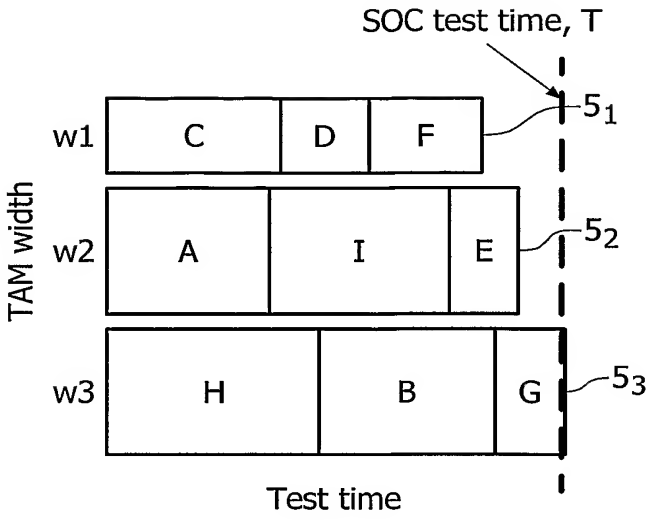

SOC test time, T
w1
C
D
F
w2
A
I
E
w3
H
B
G
TAM width
Test time
5_1
5_2
5_3

FIG. 3

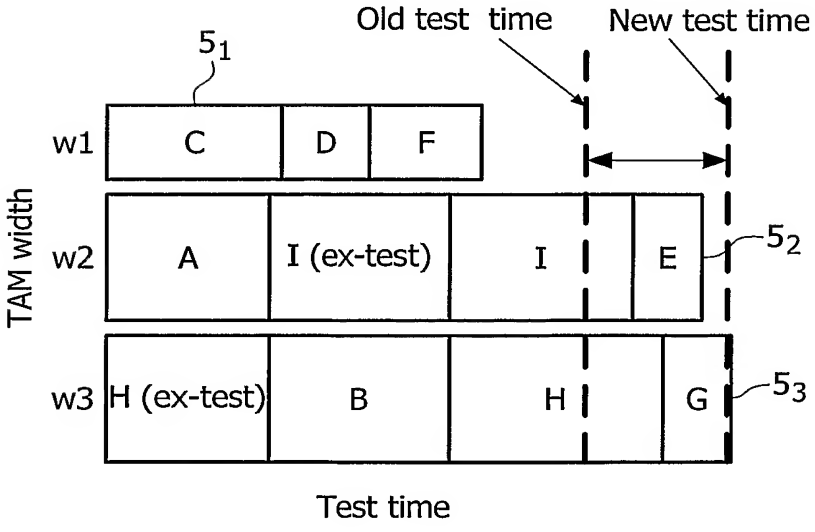

Old test time
New test time
5_1
w1
C
D
F
w2
A
I (ex-test)
I
E
w3
H (ex-test)
B
H
G
TAM width
Test time
5_2
5_3

FIG. 4

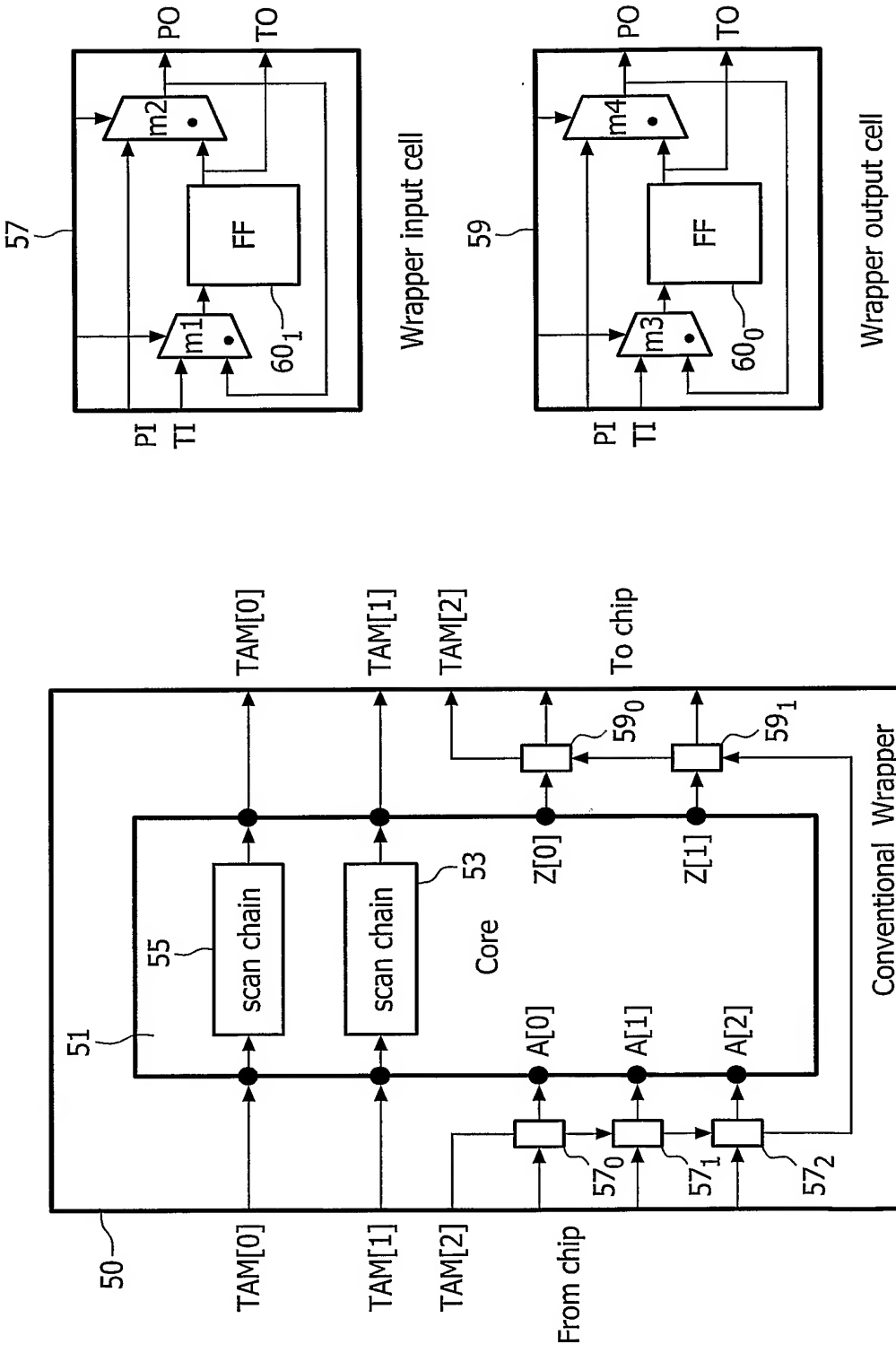

PO
TO
m2
FF
m1
60_1
57
Wrapper input cell
PI
TI
PO
TO
m4
FF
m3
60_0
59
Wrapper output cell
PI
TI
TAM[0]
TAM[1]
TAM[2]
To chip
59_0
59_1
scan chain
scan chain
53
Core
Z[0]
Z[1]
55
51
A[0]
A[1]
A[2]
Conventional Wrapper
57_0
57_1
57_2
50
TAM[0]
TAM[1]
TAM[2]
From chip

FIG. 5

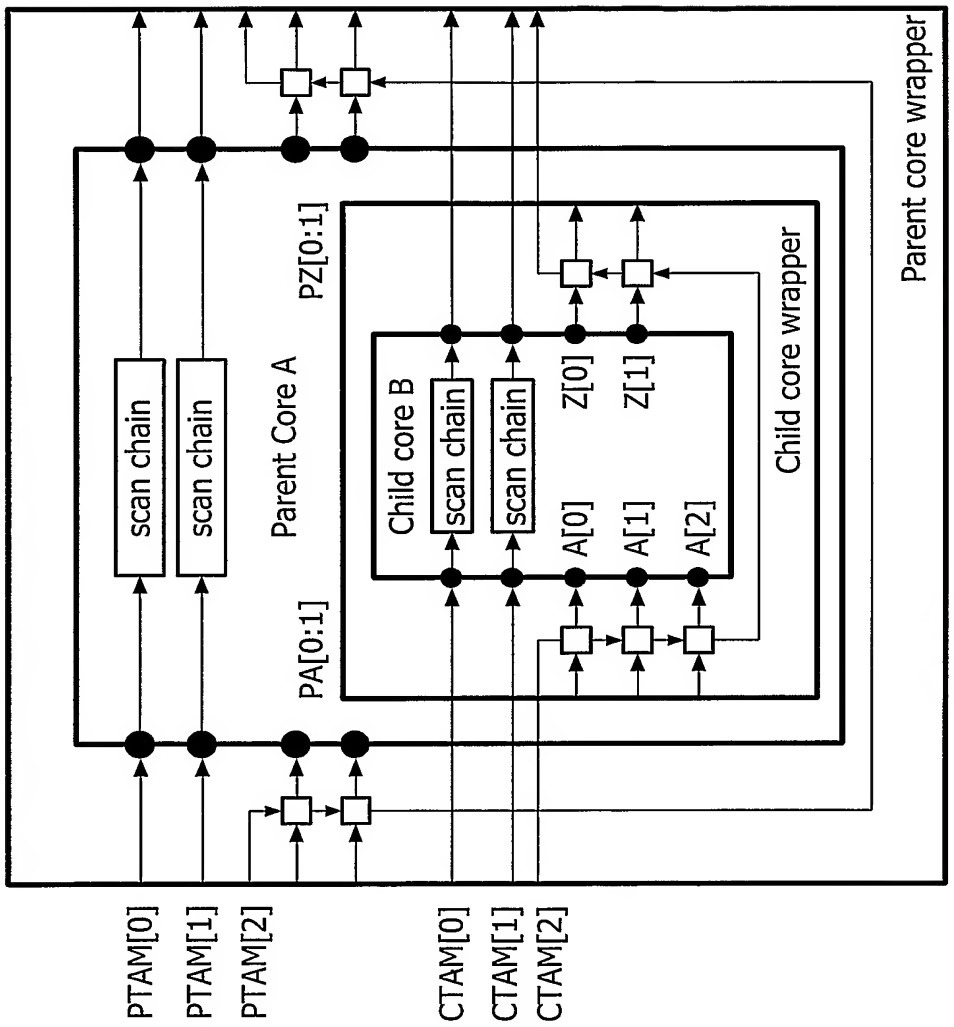

Parent core wrapper
Child core wrapper
Parent Core A
Child core B
scan chain
scan chain
scan chain
scan chain
PZ[0:1]
PA[0:1]
Z[0]
Z[1]
A[0]
A[1]
A[2]
PTAM[0]
PTAM[1]
PTAM[2]
CTAM[0]
CTAM[1]
CTAM[2]

FIG. 6

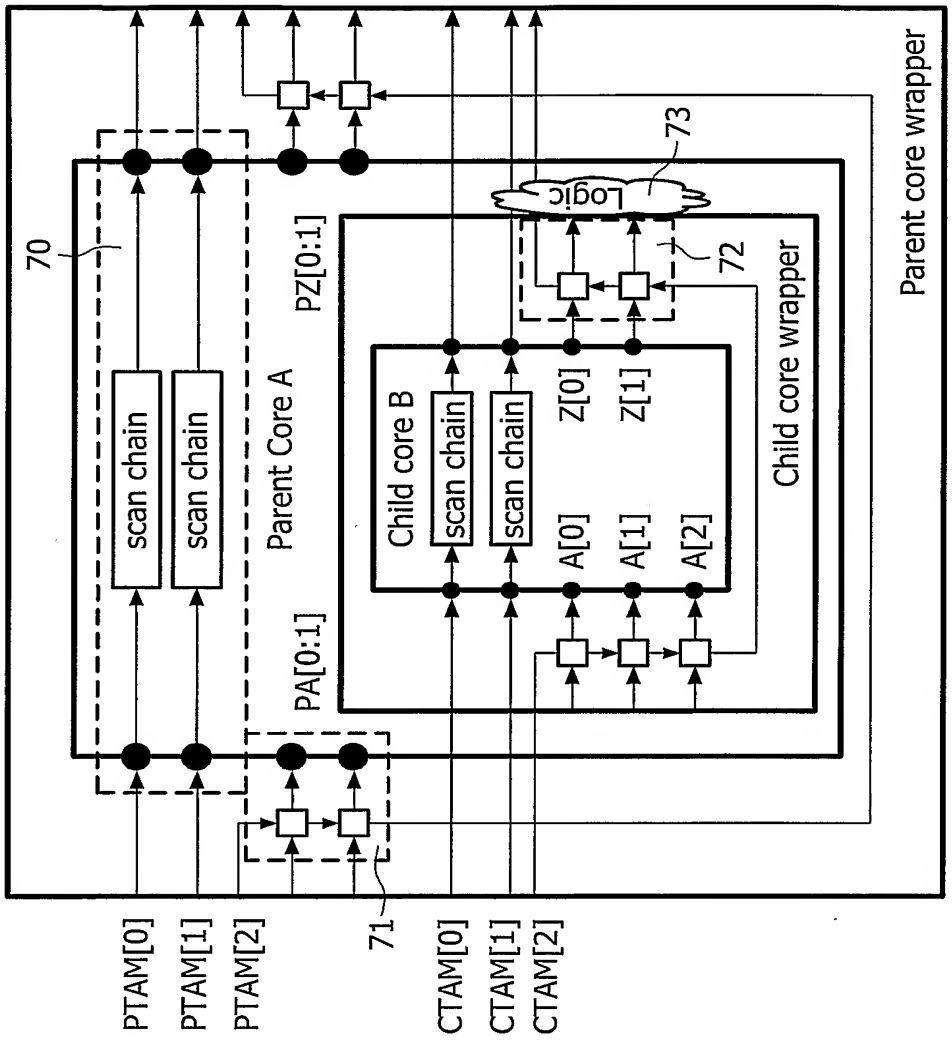

Parent core wrapper
Child core wrapper
Parent Core A
Child core B
scan chain
scan chain
scan chain
scan chain
logic
70
71
72
73
PZ[0:1]
PA[0:1]
Z[0]
Z[1]
A[0]
A[1]
A[2]
PTAM[0]
PTAM[1]
PTAM[2]
CTAM[0]
CTAM[1]
CTAM[2]

FIG. 7

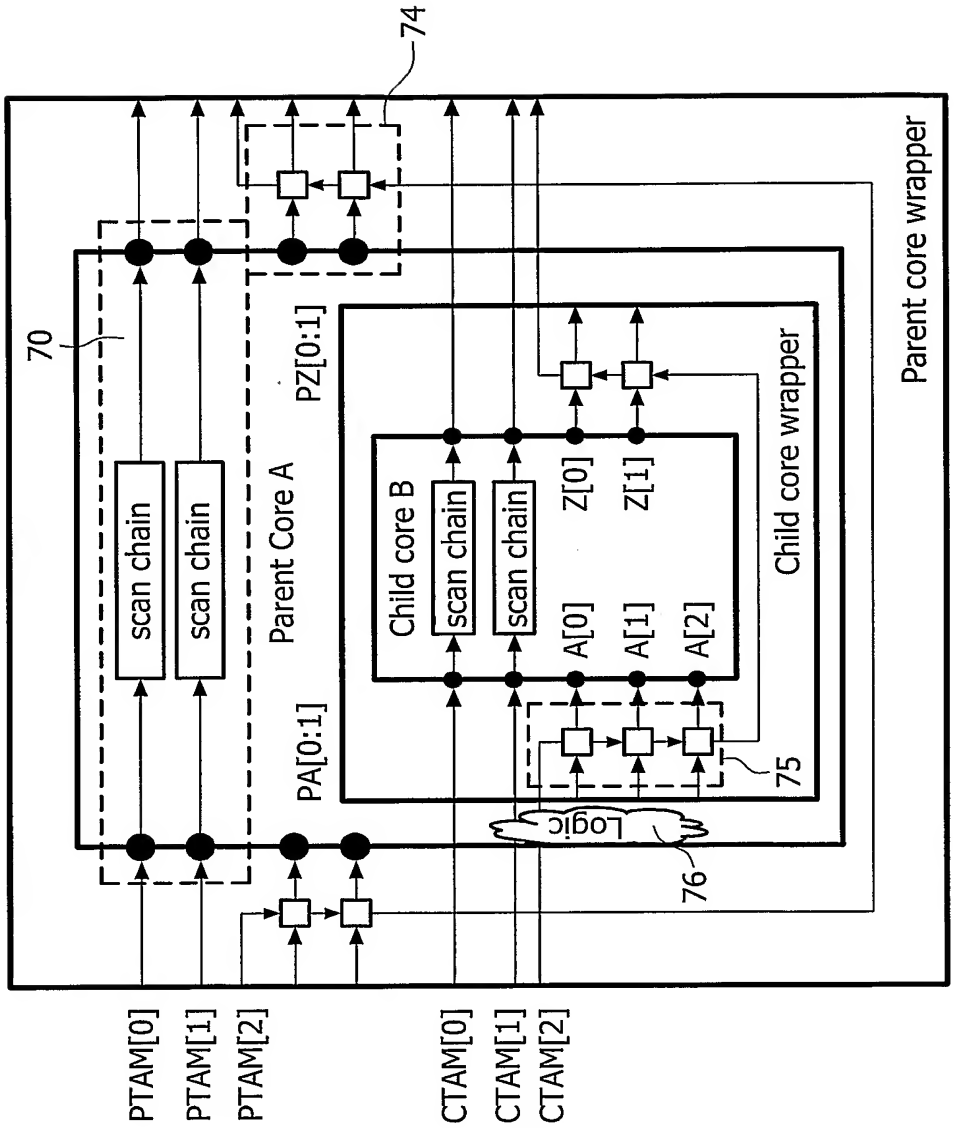

74
70
Parent core wrapper
scan chain
scan chain
Parent Core A
PZ[0:1]
PA[0:1]
Child core B
scan chain
scan chain
Z[0]
Z[1]
A[0]
A[1]
A[2]
Child core wrapper
75
Logic
76
PTAM[0]
PTAM[1]
PTAM[2]
CTAM[0]
CTAM[1]
CTAM[2]

FIG. 8

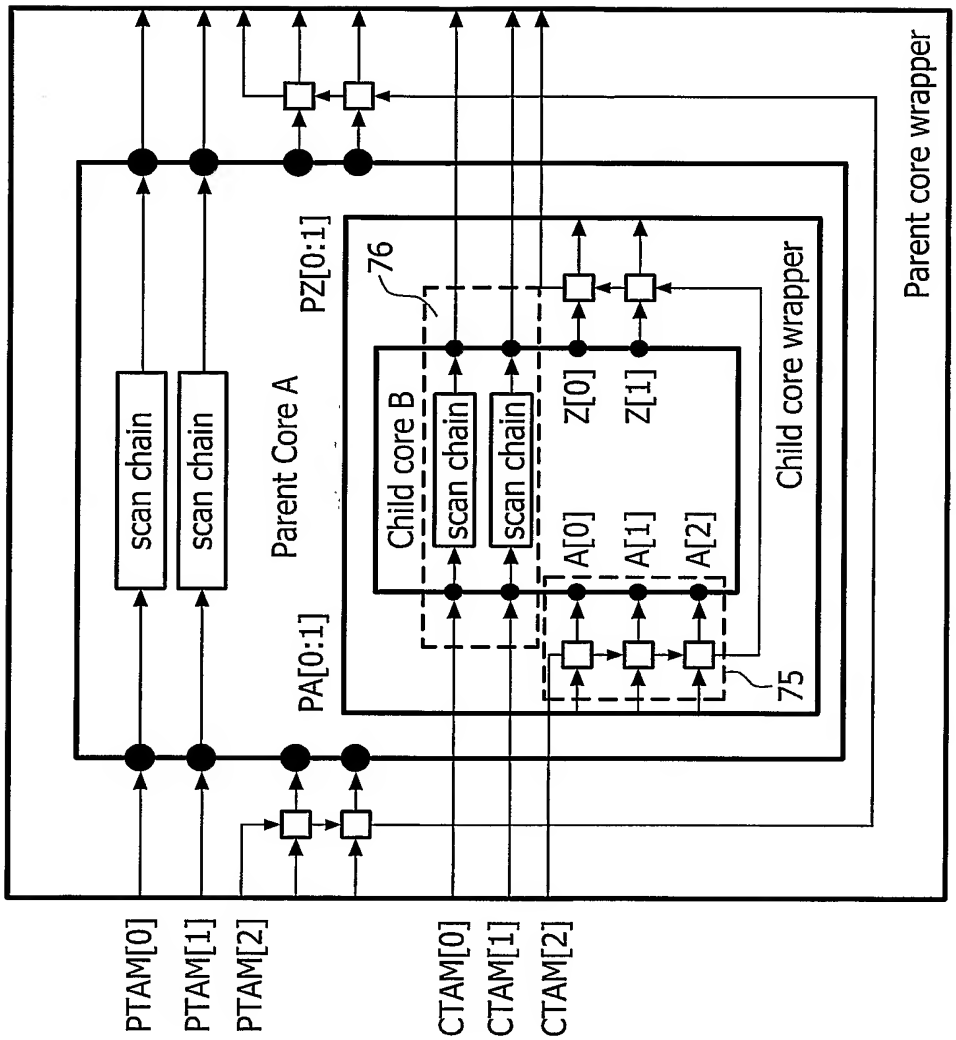

Parent core wrapper
Child core wrapper
Parent Core A
Child core B
scan chain
scan chain
scan chain
scan chain
PZ[0:1]
PA[0:1]
76
75
Z[0]
Z[1]
A[0]
A[1]
A[2]
PTAM[0]
PTAM[1]
PTAM[2]
CTAM[0]
CTAM[1]
CTAM[2]

FIG. 9

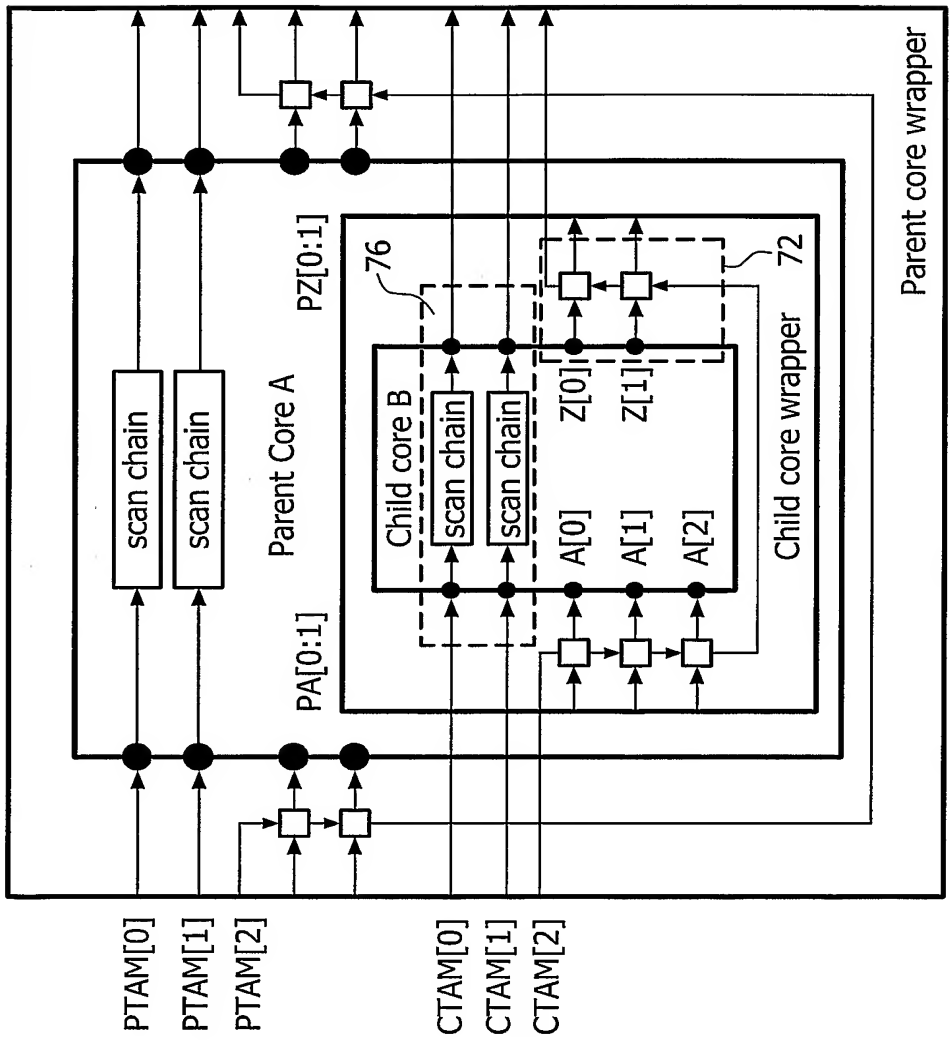

Parent core wrapper
Child core wrapper
72
76
Child core B
Parent Core A
scan chain
scan chain
scan chain
scan chain
PZ[0:1]
PA[0:1]
A[0]
A[1]
A[2]
Z[0]
Z[1]
PTAM[0]
PTAM[1]
PTAM[2]
CTAM[0]
CTAM[1]
CTAM[2]

FIG. 10

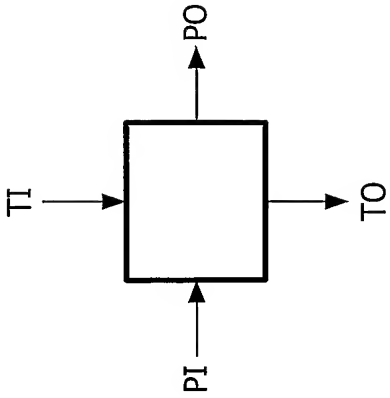


FIG. 12a

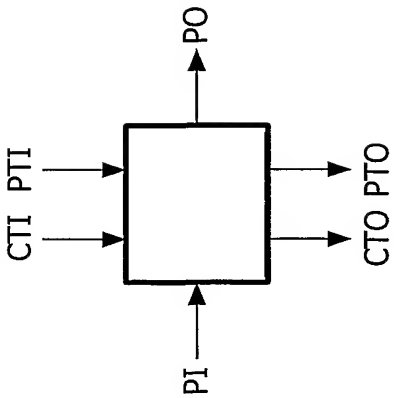


FIG. 12b

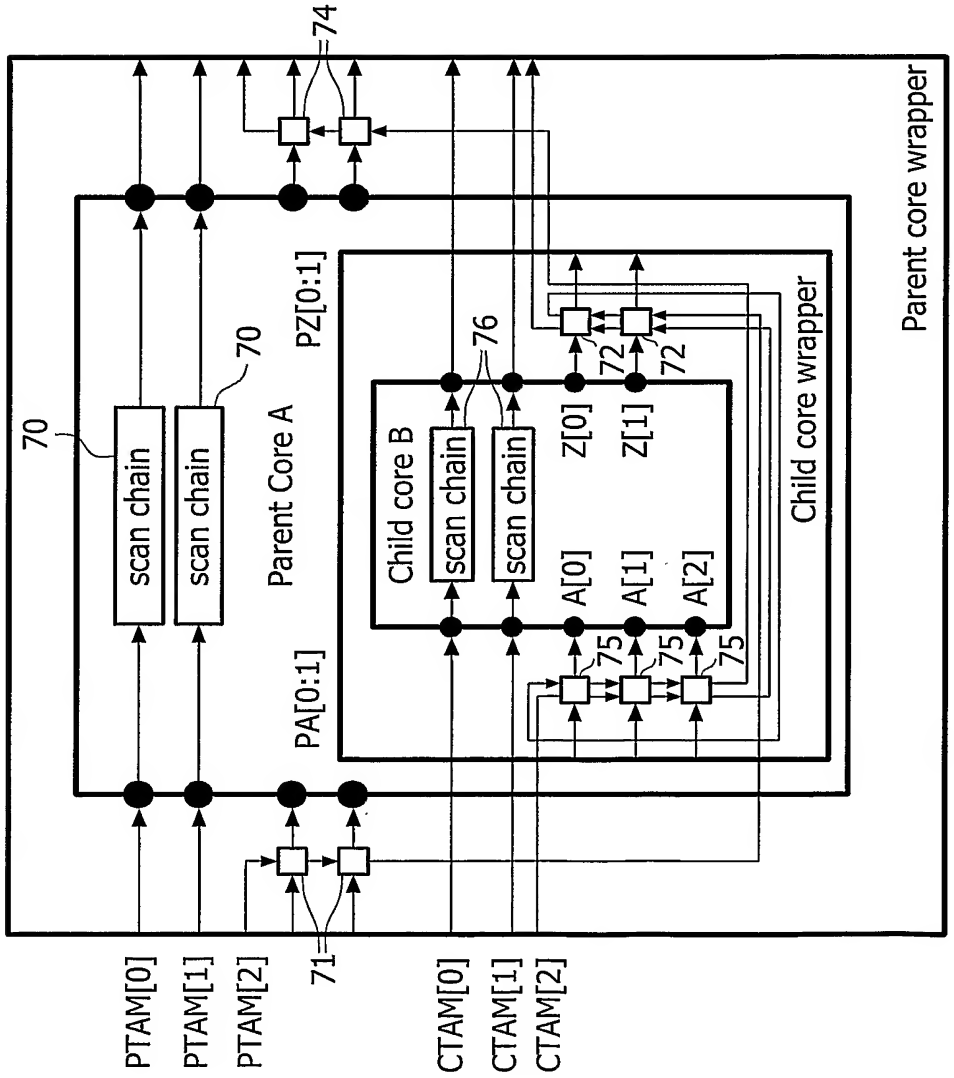
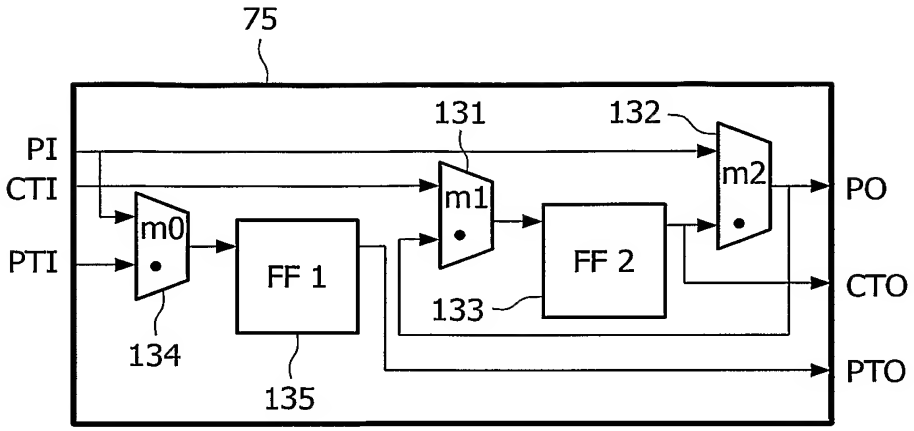
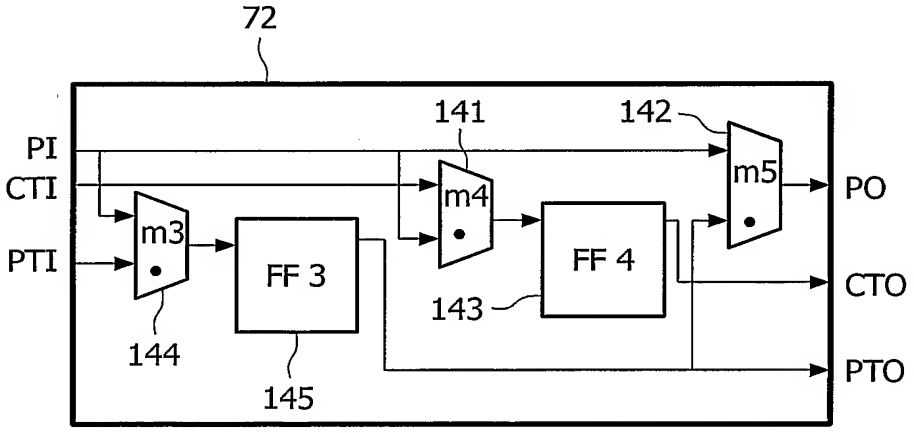


FIG. 11



Wrapper input cell

FIG. 13



Wrapper output cell

FIG. 14

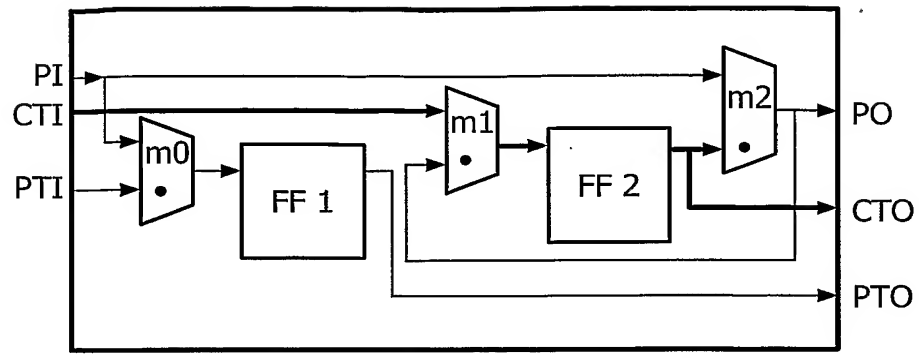


FIG. 15a

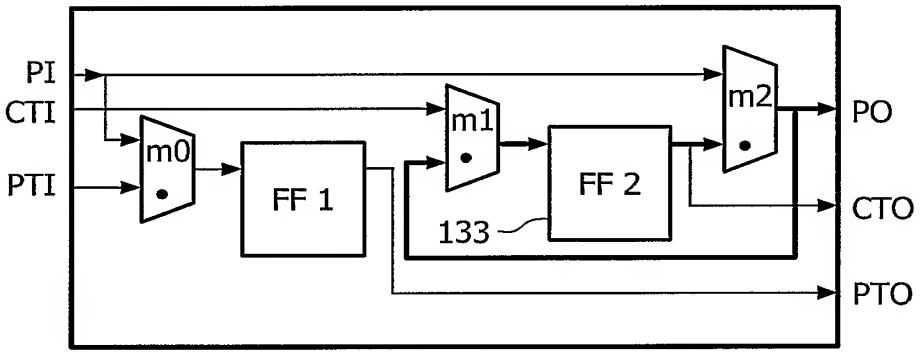


FIG. 15b

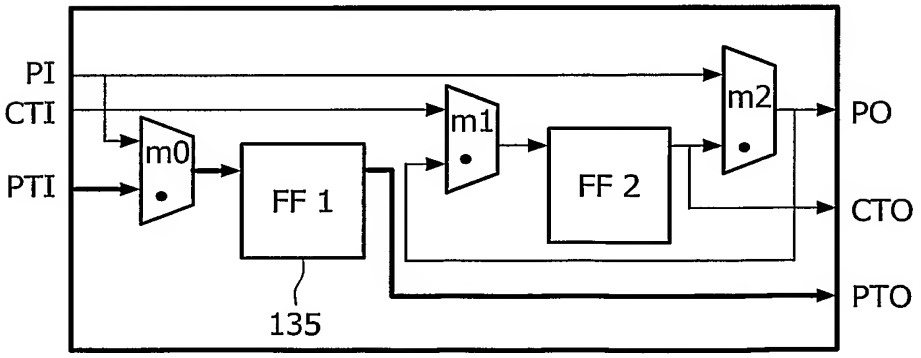


FIG. 15c

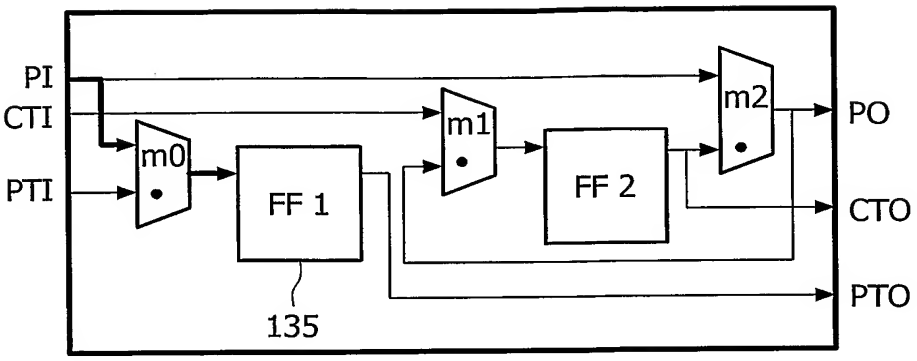


FIG. 15d

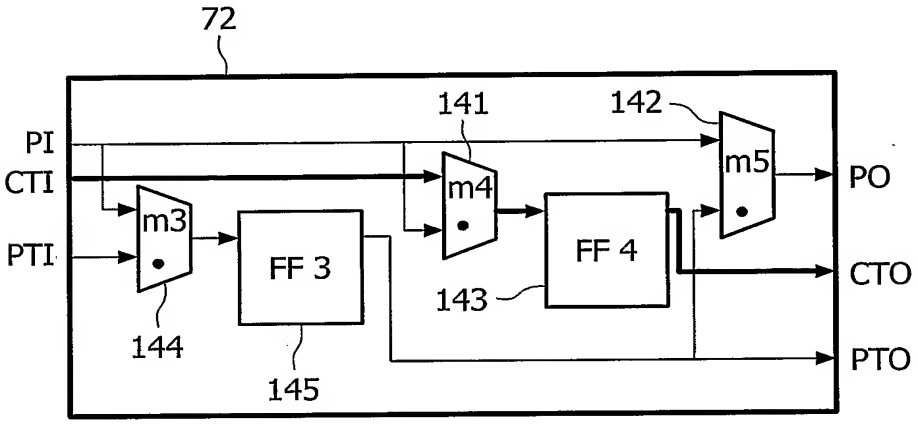


FIG. 16a

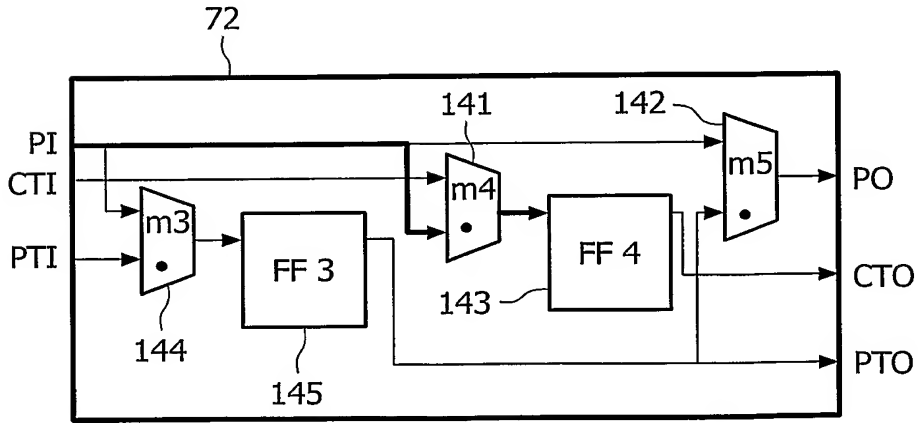


FIG. 16b

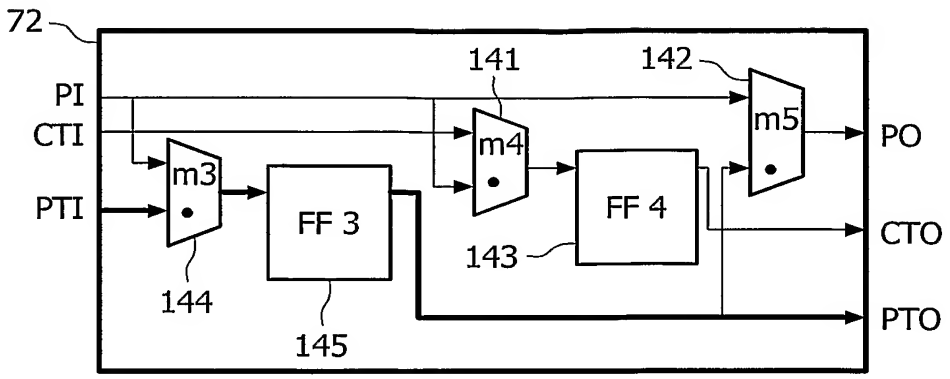


FIG. 16c

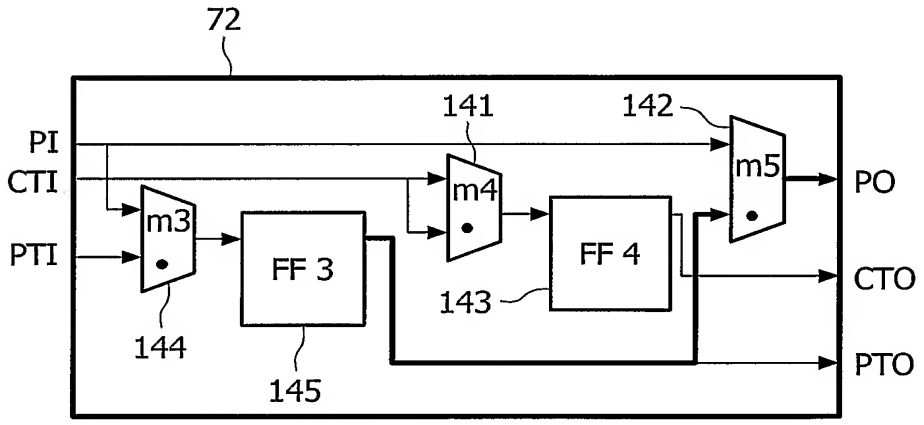


FIG. 16d

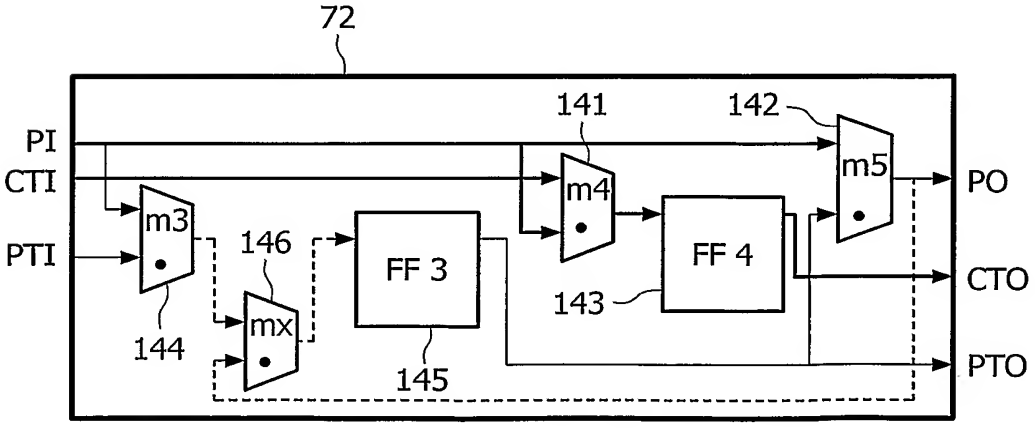


FIG. 17

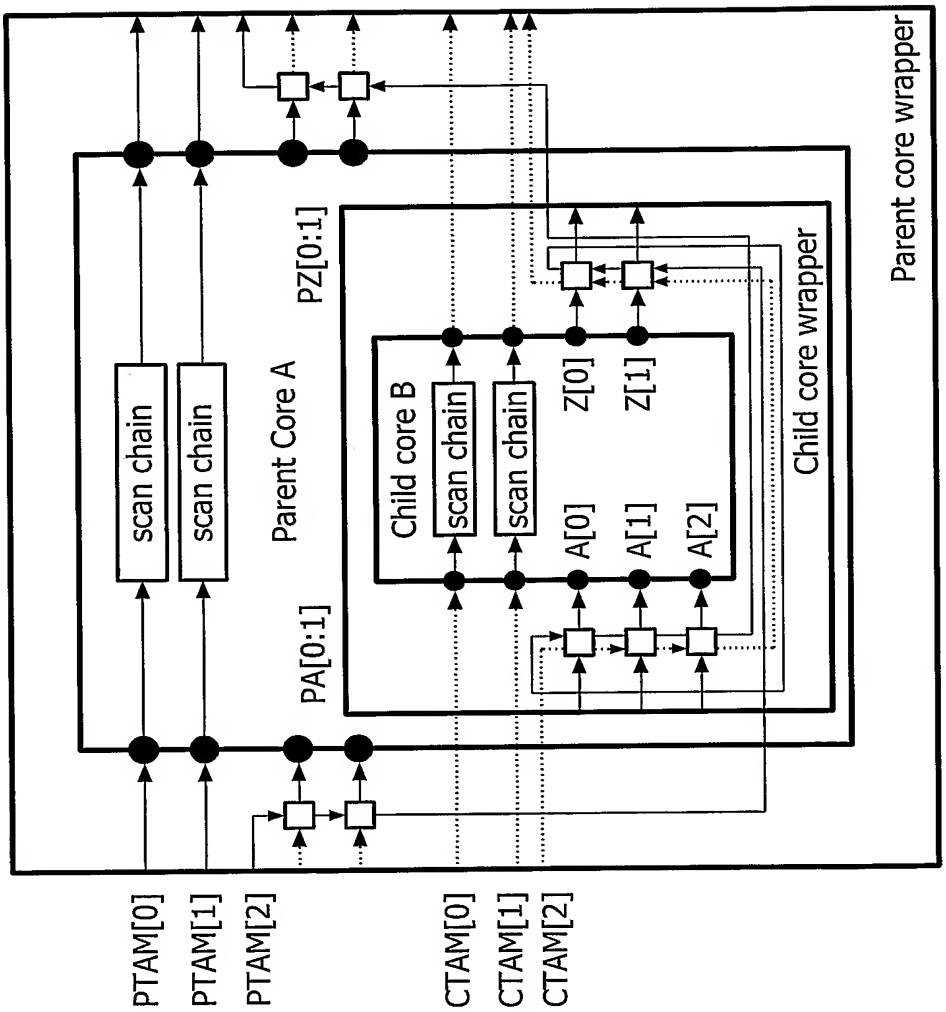

Parent core wrapper
Child core wrapper
Child core B
Parent Core A
scan chain
scan chain
scan chain
scan chain
PZ[0:1]
PA[0:1]
Z[0]
Z[1]
A[0]
A[1]
A[2]
PTAM[0]
PTAM[1]
PTAM[2]
CTAM[0]
CTAM[1]
CTAM[2]

FIG. 18a

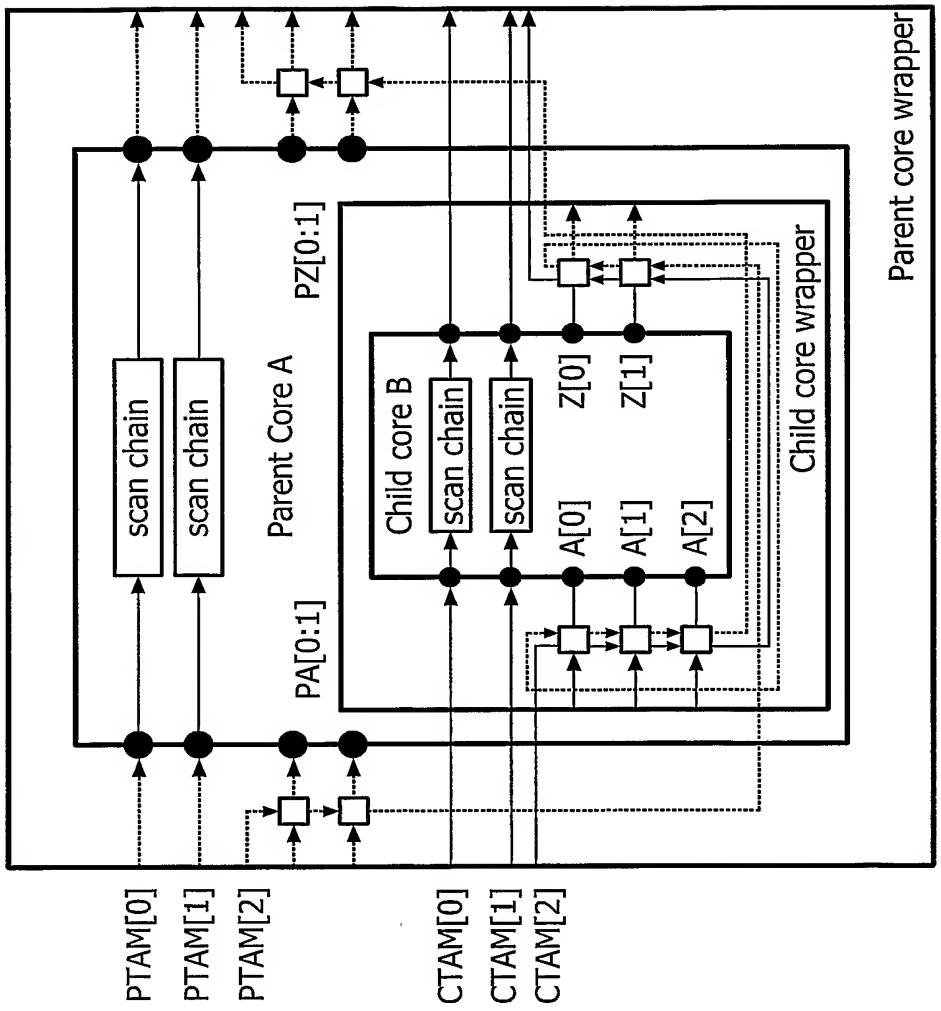

Parent core wrapper
Child core wrapper
Child core B
Parent Core A
scan chain
scan chain
scan chain
scan chain
PZ[0:1]
PA[0:1]
Z[0]
Z[1]
A[0]
A[1]
A[2]
PTAM[0]
PTAM[1]
PTAM[2]
CTAM[0]
CTAM[1]
CTAM[2]

FIG. 18b

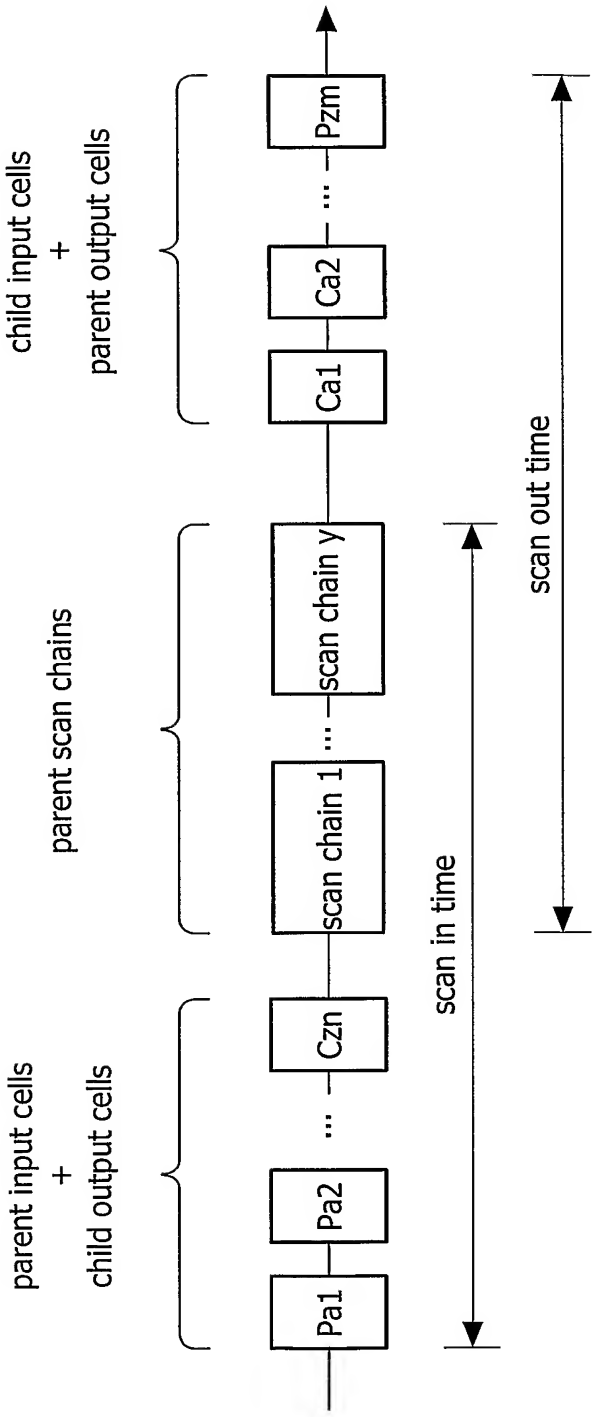

parent input cells
+
child output cells
child input cells
+
parent output cells
parent scan chains
Pa1
Pa2
...
Czn
scan chain 1
...
scan chain y
Ca1
Ca2
...
Pzm
scan in time
scan out time

FIG. 19